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PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Serial No. 09/697,305	)	Confirmation No. 4222
	)	
In re Application of	)	Group Art Unit: 2133
	)	
Takaki YOSHIDA et al.	)	Examiner: Joseph D. Torres
	)	
Filed: October 27, 2000	)	

For: FAULT DETECTING METHOD AND LAYOUT METHOD FOR SEMICONDUCTOR  
INTEGRATED CIRCUIT

REQUEST FOR ACKNOWLEDGMENT OF INFORMATION DISCLOSURE STATEMENT

U.S. Patent and Trademark Office  
Customer Service Window  
Randolph Building  
401 Dulany Street  
Alexandria, Virginia 22313-1450

Sir:

Applicants respectfully request the U.S. Patent and Trademark Office to acknowledgment receipt and consideration of the Information Disclosure Statement filed December 2, 2003. It is also respectfully requested the Examiner return an initialed copy of the PTO-1449 filed with the IDS as acknowledgment thereof.

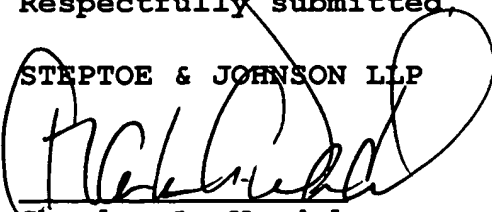
The Examiner is requested to telephone the undersigned should there be any questions regarding this matter.

Date: February 28, 2006

Respectfully submitted,

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